REMARKS

The Examiner objected to claim 1 stating: "Claim 1 is objected to because of the following informalities: In claim 1: "couples a first respective bitline or to a second respective bitline" apparently should be "couples to a first respective bitline or to a second respective bitline". Appropriate correction is required."

In response, Applicants have amended claim 1 to correct the informality in claim 1..

The Examiner rejected claims 1-20 under 35 U.S.C. 103 as being unpatentable over Yamagata et al (US 5,319,589) in view of Murakami et al. (US. 5, 134,585).

Applicants respectfully traverse the §103 rejections with the following arguments.

35 USC § 103 Rejections

As to claim 1-20, the Examiner states that: "Yamagata discloses a content-addressable memory with bitline replacement that uses a non-adjacent spare adjacent bitline. Referring to Fig. 16 of Yamagata, a "coupling circuit" 10 for coupling bitlines (DTO-DT35, DTS), and their complements, to data lines (100-1035) is controlled by a "steering signal" (400-435) for each data line. Yamagata's "coupling circuit", in operation, "couples (to) a first respective bitline or to a second respective bitline based on a steering signal", however Yamagata's "first bitline" and the replacement "second bitline" (DTS) are non-adjacent, except in the case of one bitline (DT35). Yamagata further shows a circuit (500-535, 5S) that "maintains said first respective bitline at a desired potential after said data line is coupled to said second bitline" so that a faulty unselected bitline does not introduce noise in reading. Yamagata's bitline coupling selection signals (NED) are controlled (Fig. 18) by a combination of fuse (46) and latch (47), thereby providing "fuse latches".

Murakami discloses a memory array with bitline replacement using adjacent bitlines (Figs. 11 a, 11 b), which is a well-known functional equivalent alternative to using a non-adjacent spare bitline for bitline replacement. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Yamagata's memory chip by replacing the non-adjacent bitline sparing with Murakami's adjacent bitline sparing. Such a substitution would have been obvious because Murakami's adjacent bitline sparing was already a well-known functional equivalent alternative."

First, Applicants contend that claim 1 is not obvious in view of Yamagata et al. in view of Murakami et al. because Yamagata et al. in view of Murakami et al does not teach or suggest every feature of claim 1. For example, Yamagata et al. in view of Murakami et al. does not teach or suggest "said second respective bitline being adjacent to said first respective bitline." Applicants point out that the combination of Yamagata et al. and Murakami et al. does not result in Applicants invention. In Murahmi et al. FIGs. 11A and 11B, Column Ci-1 is adjacent to column Ci, column Ci is adjacent to column Ci+1, column Ci+2 is adjacent to column Ci+1, etc. Column Ci+2 is not adjacent to column Ci, column Ci+1 intervening. In Murahami et al. FIG. 11A, before implementing redundancy, output signal line Yi-1 is connected to column Ci-1 and output signal line Yi is connected to column Ci. In Murakami et al. FIG. 11B, after implementing redundancy, output signal line Yi-1 is still connected to column Ci-1 but output signal line Yi is now connected to column Ci+2 which is not adjacent to column Ci. The "first respective bitline" (Ci) has not been replaced with the adjacent "second bitline" (Ci+1) but with non-adjacent bitline Ci+2. Thus the limitation of Applicants claim 1, namely "said second respective bitline being adjacent to said first respective bitline" is not met by the combination of Yamagata et al. and Murakami et al.

Second, Applicants traverse the Examiners statement that "bitline replacement using adjacent bitlines (Figs. 11a, and 11b), which are "well-known functional equivalent alternatives to using a non-adjacent spare bitline replacement" and request the Examiner provide evidence of the Examiners assertion under MPEP 2144.03C.

Based on the preceding arguments, Applicants respectfully maintain that claim 1 is not unpatentable over Yamagata et al. in view of Murakami et al and is in condition for allowance. Since claims 2-8 depend from claim 1, Applicants respectfully maintain that claims 2-8 are likewise in condition for allowance.

Applicants maintain that the arguments given *supra* in regards to claim 1 are applicable to claim 9. Therefore, Applicants contend that claim 9 is not obvious in view of view of Yamagata et al. in view of Murakami et al.

Based on the preceding arguments, Applicants respectfully maintain that claim 9 is not unpatentable over Yamagata et al. in view of Murakami et al. and is in condition for allowance. Since claims 10-16 depend from claim 9, Applicants respectfully maintain that claims 10-16 are likewise in condition for allowance.

Applicants contend that claim 17 is not obvious in view of view of Yamagata et al. in view of Murakami et al. because view of Yamagata et al. in view of Murakami et al. does not teach or suggest every feature of claim 17. For example, Yamagata et al. in view of Murakami et al. does not teach or suggest "means for directing a first respective read line coupled to said first respective bitline to a second respective read line coupled to said second respective bitline in response to said steering signal." Applicants respectfully point out that Yamagata et al. and Murakami et al. are silent as to redirection of read lines.

Further, Applicants maintain that the arguments given *supra* in regards to claim 1 are applicable to claim 17.

Based on the preceding arguments, Applicants respectfully maintain that claim 17 is not unpatentable over Yamagata et al. in view of Murakami et al. and is in condition for allowance. Since claims 18-20 depend from claim 17, Applicants respectfully maintain that claims 18-20 are likewise in condition for allowance

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that claims 1-20 meet the acceptance criteria for allowance and therefore request favorable action. If Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invite the Examiner to contact the Applicants' representative at the telephone number listed below. The Director is hereby authorized to charge and/or credit Deposit Account 09-0456.

Respectfully submitted,
FOR:
Batson et al.

BY: Jack P Friedman
Jack P. Friedman
Reg. No. 44,688
FOR:
Anthony M. Palagonia
Registration No.: 41,237

Dated: 11/01/2004

3 Lear Jet Lane, Suite 201
Schmeiser, Olsen & Watts
Latham, New York 12110
(518) 220-1850
Agent Direct Dial Number: (802)-899-5460